UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,352	08/07/2002	Gilbert Wolrich	10559-308US1	7931

7590 09/30/2005

Fish & Richardson
225 Franklin Street
Boston, MA 02110-2804

EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/069,352	WOLRICH ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *all up to12/13/04* .
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-38 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as received on 2/22/2002, Power of Attorney and Extension of Time as received on 8/7/2002, IDS as received on 6/4/2004, IDS (4x) as received on 12/5/2004, and IDS as received on 12/13/2004.

Specification

3. The abstract of the disclosure is objected to because the examiner does not feel that it describes the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. All that the abstract appears to say is that applicant has a multithreaded system with a load instruction. It is asked that applicant further elaborate on the specifics of the invention while keeping it to less than 150 words. Correction is required. See MPEP § 608.01(b).

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Regarding claims 7 and 26, the examiner has been unable to find anything in the specification regarding a breakpoint register (while BP2 and BP0 have been mentioned in the specification, this does not necessarily refer to a breakpoint register).

5. The disclosure is objected to because of the following informalities:

* On page 3, line 9, replace "16b" with --26b--.

* On page 3, line 12, remove the large space after "cause".

* On page 8, lines 25-26, reference number 72c from Fig.3 does not appear to point to a counter.

* On page 10, the examiner does not understand the sentence stretching from lines 28-30, as it does not appear to be grammatically correct. Please reword the sentence.

Appropriate correction is required.

Drawings

6. The informal drawings are not of sufficient quality to permit examination (especially Fig.2 and Fig.3). Accordingly, replacement drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to this Office action. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action.

Applicant is given a TWO MONTH time period to submit new drawings in compliance with 37 CFR 1.81. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a). Failure to timely submit replacement drawing sheets will result in ABANDONMENT of the application.

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

Reference number 16c in Fig.1.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

8. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

In Fig.3, component 72d.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

9. The drawings are objected to because of the following minor informalities:

In Fig.1, the text in component 30 is unclear. Also, modify "16a" so that it is legible. Also, component 26a should say "SDRAM Controller" (not "memory unit") and component 26b should say "SRAM Controller" (not "SRAM Unit").

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

10. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. The examiner is unable to find the majority of the claimed subject matter in the drawings. Therefore, the subject matter of claims 1-5, 7-24, and 26-38 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

11. Claim 3 is objected to because of the following informalities: For consistency, please replace "status and control register " with --control and status register--. Also, replace "in contained" with --is contained--. Appropriate correction is required.

12. Claim 5 is objected to because the it appears to be grammatically incorrect. Please reword the claim so that it is more clear. Appropriate correction is required.

13. Claim 7 is objected to because of the following informalities: Insert --a-- before "second". Also, the phrase "The method of claim 1 shifting comprises:" is grammatically incorrect. Appropriate correction is required.

14. Claim 11 is objected to because of the following informalities: Replace "an micro" with --a micro--. Appropriate correction is required.

15. Claim 22 is objected to because of the following informalities: For consistency, please replace "status and control register " with --control and status register--. Appropriate correction is required.

16. Claim 24 is objected to because the it appears to be grammatically incorrect. Please reword the claim so that it is more clear. Appropriate correction is required.

17. Claim 30 is objected to because of the following informalities: Replace "an micro" with --a micro--. Appropriate correction is required.

18. Claim 38 is objected to because it includes the abstract. Please remove the abstract from claim 38. Appropriate correction is required.

Claim Rejections - 35 USC § 112

19. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

20. Claims 7 and 26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant

art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is not clear to the examiner what exactly applicant is trying to accomplish with respect to claims 7 and 26. Claim 1 states that data is received and stored. Claim 7 then states shifting a first portion of the data and shifting a second portion of the data into a BP register. However, nowhere in the specification does it state that after the data is stored, a first portion of it is shifted and a second portion is shifted into a BP register. Is the data shifted after the data is stored or is it shifted before the data is stored? Applicant does not appear to have support in the specification for the former but that is what is claimed. Is non-shifted data ever loaded into the CSR, which is what is claimed in claim 1, for instance? Applicant needs to clarify claims 1, 7, 20, and 26. The examiner's interpretation of the claims in question will be evident in the rejections below.

21. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

22. Claims 3-4, 7, 22-23, and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

23. Claims 3 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More specifically, it is not clear how a register is contained in a bus. That is, how is a hardware register contained in a set of wires? The examiner assumes that

applicant meant that the register is coupled to the bus and therefore will interpret the claim in such a fashion.

24. Claims 7 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More specifically, it is not clear what applicant means by shifting data into a BP register 2 to a BP register 0 because the examiner is unaware of what a BP register 2 or a BP register 0 is. What do these numbers represent?

Claim Rejections - 35 USC § 102

25. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

26. Claims 1-6, 8-10, 20-25, and 27-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen, U.S. Patent No. 6,058,465 (as disclosed by applicant).

27. Referring to claim 1, Nguyen has taught a method of operating a processor comprising receiving data in a processing thread having a processing thread number and loading the data into a register having a register address corresponding to the processing thread number. See columns 91-92, and note the VCHGCR instruction which is executed by one of multiple threads (column 4, lines 33-36). If multiple threads exist, then there exists a first thread, second thread,

etc (they are numbered). Note from columns 91-92 that data is loaded into the addressable VCSR register (in the CBANK, SMM, and CEM bits). For data to be loaded, it must first be received. For instance, in order to clear a bit, a 0 must be received. In order to set a bit, a 1 must be received. Since the instruction is executed by a thread, everything involved with the instruction corresponds to that particular thread.

28. Referring to claim 2, Nguyen has taught a method as described in claim 1. Nguyen has further taught that the register is a control and status register. See columns 91-92 and note that the register is a control register with status bits which dictate operation.

29. Referring to claim 3, Nguyen has taught a method as described in claim 2. Nguyen has further taught that the control and status register is coupled to a 64-bit wide first-in first-out (FIFO) bus. See Fig.1, and note the 64-bit bus coupled to component 158 which is further coupled to the rest of the system. The bus is inherently FIFO because data that is sent over the bus at time A will arrive at its destination before data that is sent over the bus at time B (where B > A).

30. Referring to claim 4, Nguyen has taught a method as described in claim 3. Nguyen has further taught that the FIFO bus interfaces with Media Access Controller (MAC) Devices. See column 1, lines 36-40 and note that the invention is concerned with multimedia applications. Therefore, it would be coupled to a media access controller.

31. Referring to claim 5, Nguyen has taught a method as described in claim 1. Nguyen has further taught that the data represents values hexadecimal mask 0 to hexadecimal mask 0x3FF. Note from columns 91-92 that the data written to the register may be either 0 (when clearing a bit) or 1 (when setting a bit). Consequently, the data represents values in the range 0 to 3FF.

32. Referring to claim 6, Nguyen has taught a method as described in claim 1. Nguyen has further taught that the processing thread represents processing in a micro engine of a multithreaded processor. Again, see column 4, lines 33-36.

33. Referring to claim 8, Nguyen has taught a method as described in claim 1. Nguyen has further taught that receiving the data further comprises receiving a token. See columns 91-92 and note that receiving the data to be written to the control register must be preceded by receiving the VCHGCR instruction (token). Therefore, the receiving of the data is coupled with receiving the token.

34. Referring to claim 9, Nguyen has taught a method as described in claim 8. Nguyen has further taught that the token represents overriding qualifiers. Since the instruction writes to a control register using the data provided in the instruction, the data represents overriding qualifiers as everything already in the control register will be overridden by new data to be written.

35. Referring to claim 10, Nguyen has taught a method as described in claim 8. Nguyen has further taught that the token is a 32-bit word. See columns 91-92 and note the instruction (token) is 32 bits.

36. Referring to claims 20-25 and 27-29, claims 20-25 and 27-29 are rejected for the same reasons set forth in the rejection of claims 1-6 and 8-10, respectively, because Nguyen has taught instructions stored on a medium for performing the method of claims 1-6 and 8-10.

37. Claims 1-6, 8-9, 20-25, and 27-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Intel, "IA-64 Application Developer's Architecture Guide," May 1999 (herein referred to as Intel).

38. Referring to claim 1, Intel has taught a method of operating a processor comprising:

a) receiving data in a processing thread having a processing thread number. See page 2-3, section 2.4 and note that multiple threads may be executed. A given thread may include a shift instruction (page 7-165) in which shifted data is obtained. Note that the thread which includes this instruction would include a thread number (shift amount).

b) loading the data into a register having a register address corresponding to the processing thread number. From page 7-165, the shifted data is stored in a specified register which corresponds to the thread number (shift amount). More specifically, every item (destination, source, shift amount, opcode, predicate) in the shift left instruction corresponds to one another.

39. Referring to claim 2, Intel has taught a method as described in claim 1. Intel has further taught that the register is a control and status register. Any register that is written to is a control/status register because when it is used in any future instruction as a source, it controls the outcome of that instruction.

40. Referring to claim 3, Intel has taught a method as described in claim 2. Intel has further taught that the control and status register is coupled to a 64-bit wide first-in first-out (FIFO) bus. See page 3-1 and note that the general purpose registers (which the shift left instruction operates on) are 64 bits wide. Consequently, 64-bit data must be able to be written to the register and therefore, a 64-bit bus exists. The bus is inherently FIFO because data that is sent over the bus at time A will arrive at its destination before data that is sent over the bus at time B (where B > A).

41. Referring to claim 4, Intel has taught a method as described in claim 3. Intel has further taught that the FIFO bus interfaces with Media Access Controller (MAC) Devices. See page 2-2 section 2.3 and note that multimedia instructions exist which would be executed my multimedia execution units. Consequently, the bus interfaces with media access controller devices.

42. Referring to claim 5, Intel has taught a method as described in claim 1. Intel has further taught that the data represents values hexadecimal mask 0 to hexadecimal mask 0x3FF. From page 7-165, the shifted data is a 64-bit number that may take on any of the values in the 64-bit range. Since 0-3FF is in the 64-bit range, the data may be a value from 0-3FF.

43. Referring to claim 6, Intel has taught a method as described in claim 1. Intel has further taught that the processing thread represents processing in a micro engine of a multithreaded processor. Again, see page 2-3, section 2.4.

44. Referring to claim 8, Intel has taught a method as described in claim 1. Intel has further taught that receiving the data further comprises receiving a token. See columns 91-92 and note that receiving the data to be written to the register must be preceded by receiving the shift instruction (token) itself. Therefore, the receiving of the data is coupled with receiving the token.

45. Referring to claim 9, Intel has taught a method as described in claim 8. Intel has further taught that the token represents overriding qualifiers. The shift amount is an overriding qualifier because if is the first thing that is performed in the operation (shifting and then storing). Consequently, shifting is the most important feature. Furthermore, a qualifying predicate (qp) is also a overriding qualifier as it will override the decision to execute the instruction and result in the non-execution.

46. Referring to claims 20-25 and 27-28, claims 20-25 and 27-28 are rejected for the same reasons set forth in the rejection of claims 1-6 and 8-9, respectively, because Intel has taught instructions stored on a medium for performing the method of claims 1-6 and 8-9.

Claim Rejections - 35 USC § 103

47. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

48. Claims 11-19 and 30-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen, as applied above.

49. Referring to claim 11, Nguyen has taught a method as described in claim 10. Nguyen has further taught that a token format comprises data in bits 31:0. Nguyen has not explicitly taught that the data in bit 31 corresponds to an OV field, the data in bits 30:28 corresponds to a micro engine (UENG) ADDR field, the data in bits 27:16 corresponds to a reserved field, the data in bit 15 corresponds to an OV field, the data in bits 14:5 corresponds to a fast write data field, the data in bits 4:3 corresponds to a reserved field, the data in bit 2 corresponds to an OV field, and the data in bits 1:0 corresponds to a CTX field. However, these differences are only found in the nonfunctional descriptive material as the dividing up of the token bits into named fields does not affect how the token data is used to control the system. For instance, bit 31 of the VCHGCR instruction has a meaning in the system whether or not it is called an OV field or not. Thus, the descriptive material will not distinguish the claimed invention from the prior art in terms of

patentability. See In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); In re Lowry, 32 F.3d 1579, 32, USPQ2d 1031 (Fed. Cir. 1994). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to call a bit or any group of bits in the token a particular type of field as it does not alter how the data controls the system.

50. Referring to claim 12, Nguyen has taught a method as described in claim 11. Nguyen has further taught that a micro engine address overrides a default micro engine address if bit 31 is set. See columns 91-92 and note that the VCHGCR instruction requires that bit 31 is set. When it is set and the VCHGCR instruction executes, bits 1:0 (address of the data to control the CBANK bit) will override the CBANK bit (which is bit address). For instance, if the CBANK bit is defaulted to 1, then if bits 1:0 of the instruction are 01, then the CBANK bit will be overridden such that contains zero.

51. Referring to claim 13, Nguyen has taught a method as described in claim 11. Nguyen has further taught that bits 30:28 specify a micro engine associated with a control and status register (CSR). All of the bits of the token specify a control and status register (and consequently, the engine in which the register exists). Therefore, bits 30:28 do such specification. Without these bits, the instruction would be invalid.

52. Referring to claim 14, Nguyen has taught a method as described in claim 11. Nguyen has further taught that bits 27:16 return 0 when read. That is, if bits 27:16 are all set to 0, then when read, the value 0 would be obtained.

53. Referring to claim 15, Nguyen has taught a method as described in claim 11. Nguyen has further taught that a micro engine address overrides a default micro engine address if bit 15 is

set. See columns 91-92 and note that the VCHGCR instruction's bit 15 is an undefined bit. That is, it could equal 0 or 1 and operate the same. Consequently, when bit 15 is set and VCHGCR instruction executes, bits 1:0 (address of the data to control the CBANK bit) will override the CBANK bit (which is bit address). For instance, if the CBANK bit is defaulted to 1, then if bits 1:0 of the instruction are 01, then the CBANK bit will be overridden such that contains zero.

54. Referring to claim 16, Nguyen has taught a method as described in claim 11. Nguyen has further taught that bits 5:0 represent valid data to be written to a control and status register (CSR). That is, based on the values of these bits, certain data will be written to the CSR. Nguyen has not taught that bits 14:5 represent valid data to be written to a control and status register (CSR). However, as shown in In re Rose, 105 USPQ 237 (CCPA 1955), changes in size/range are generally not given patentable weight or would have been an obvious improvement. In this case, both applicant and the prior art teach representing data to be written to a CSR. Applicant not only represents more bits, but represents bits from a different portion of the token than the prior art. The examiner asserts that this is merely a design choice and is not given patentable weight. For instance, a person of ordinary skill in the art at the time of the invention would realized that if there are more bits in a CSR in system A than in a CSR in system B, then more data needs to be written to it. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Nguyen such that bits 14:5 represent valid data for writing to a CSR.

55. Referring to claim 17, Nguyen has taught a method as described in claim 11. Nguyen has further taught that bits 4:3 return 0 when read. That is, if bits 4:3 are all set to 0, then when read, the value 0 would be obtained.

56. Referring to claim 18, Nguyen has taught a method as described in claim 11. Nguyen has further taught that a context (CTX) field overrides a default context is bit 2 is set. From columns 91-92, if bit 2 is set, the current SMM bit operation is changed from whatever it currently is to either clear or toggle operation.

57. Referring to claim 19, Nguyen has taught a method as described in claim 11. Nguyen has further taught that bits 1:0 specify a context associated with a control and status register (CSR) reference. From columns 91-92, if bits 1:0 specify the context in which the CBANK bit is modified.

58. Referring to claims 30-38, claims 30-38 are rejected for the same reasons set forth in the rejection of claims 11-19, respectively, because Nguyen has taught instructions stored on a medium for performing the method of claims 11-19.

59. Claims 7, 10-19, 26, and 29-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel as applied above.

60. Referring to claim 7, Intel has taught a method as described in claim 1. Intel has further taught:

a) shifting a first portion (the entire data) of the data by an amount equal to the processing thread number. See page 7-165 and note that data is shifted left by the thread number (shift amount).

b) Intel has taught shifting a second portion of the data into a register 2 to a register 0 (the lower three bits of a register). See page 7-165 and note the shifted data is stored in the entire destination register including bits 0-2. Intel has not taught that the register is a breakpoint register. However, these differences are only found in the nonfunctional descriptive material and

do not function how the register functions (the register stores data regardless of whether it is a breakpoint register, a general-purpose register, etc). Thus, the descriptive material will not distinguish the claimed invention from the prior art in terms of patentability. See In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); In re Lowry, 32 F.3d 1579, 32, USPQ2d 1031 (Fed. Cir. 1994). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to store any type of data in the register because the type of data does not patentably distinguish the claimed invention.

61. Referring to claim 10, Intel has taught a method as described in claim 8. Intel has further taught that the token is a 40-bit word. See page C-4, instruction I7 (shift left instruction). Intel has not taught that the token is a 32-bit word. However, as shown in In re Rose, 105 USPQ 237 (CCPA 1955), changes in size/range are generally not given patentable weight or would have been an obvious improvement. The examiner asserts that this is merely a design choice and is not given patentable weight. An instruction may be all different sizes depending on the architecture on which it is to execute. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Nguyen such that the shift left token is 32-bits.

62. Referring to claim 11, Intel has taught a method as described in claim 10. Intel has further taught that a token format comprises data in bits 31:0. See page C-4 (instruction I7). Intel has not explicitly taught that the data in bit 31 corresponds to an OV field, the data in bits 30:28 corresponds to a micro engine (UENG) ADDR field, the data in bits 27:16 corresponds to a reserved field, the data in bit 15 corresponds to an OV field, the data in bits 14:5 corresponds to a fast write data field, the data in bits 4:3 corresponds to a reserved field, the data in bit 2

corresponds to an OV field, and the data in bits 1:0 corresponds to a CTX field. However, these differences are only found in the nonfunctional descriptive material as the dividing up of the token bits into named fields does not affect how the token data is used to control the system. For instance, bit 31 of the VCHGCR instruction has a meaning in the system whether or not it is called an OV field or not. Thus, the descriptive material will not distinguish the claimed invention from the prior art in terms of patentability. See In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); In re Lowry, 32 F.3d 1579, 32, USPQ2d 1031 (Fed. Cir. 1994). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to call a bit or any group of bits in the token a particular type of field as it does not alter how the data controls the system.

63. Referring to claim 12, Intel has taught a method as described in claim 11. Intel has further taught that a micro engine address overrides a default micro engine address if bit 31 is clear. See page C-23 (C.3.1.7) and note that when bit 31 is 0 and a shift left occurs, data from one engine address (register) is shifted and used to override data at another engine address (another register). Intel has not taught that such action occurs when bit 31 is set. However, the examiner asserts that this is an obvious design choice modification. The instruction would work just as well if bit 31 was set and no other instructions conflicted with it. As a result, since the functionality of applicant's claimed invention and the prior art are already the same, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify bit 31 of the token to be set.

64. Referring to claim 13, Intel has taught a method as described in claim 11. Intel has further taught that bits 30:28 specify a micro engine associated with a control and status register

(CSR). All of the bits of the token specify a control and status register (and consequently, the engine in which the register exists). Therefore, bits 30:28 do such specification. Without these bits, the instruction would be invalid.

65. Referring to claim 14, Intel has taught a method as described in claim 11. Intel has further taught that bits 27:16 return 0 when read. That is, if bits 27:16 are all set to 0, then when read, the value 0 would be obtained.

66. Referring to claim 15, Intel has taught a method as described in claim 11. Intel has further taught that a micro engine address overrides a default micro engine address if bit 15 is set. See page C-4 and note that if bit 15 is set (which it may be as it's part the source register field, then the default register (destination register with current value) will be overridden with a new register address (source register which supplies the shifted data).

67. Referring to claim 16, Intel has taught a method as described in claim 11. Intel has further taught that bits 26:13 represent valid data to be written to a control and status register (CSR). See page C-4 (I7). That is, based on the values of these bits, certain data will be written to the CSR. Intel has not taught that bits 14:5 represent valid data to be written to a control and status register (CSR). However, as shown in In re Rose, 105 USPQ 237 (CCPA 1955), changes in size/range are generally not given patentable weight or would have been an obvious improvement. In this case, both applicant and the prior art teach representing data to be written to a CSR. Applicant not only represents less bits, but represents bits from a different portion of the token than the prior art. The examiner asserts that this is merely a design choice and is not given patentable weight. For instance, a person of ordinary skill in the art at the time of the invention would realized that if there are less bits in a CSR in system A than in a CSR in system

B, then less data needs to be written to it. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Nguyen such that bits 14:5 represent valid data for writing to a CSR.

68. Referring to claim 17, Intel has taught a method as described in claim 11. Intel has further taught that bits 4:3 return 0 when read. That is, if bits 4:3 are all set to 0, then when read, the value 0 would be obtained.

69. Referring to claim 18, Intel has taught a method as described in claim 11. Intel has further taught that a context (CTX) field overrides a default context is bit 2 is set. See page C-4 and note that if bit 2 is set, a certain qualifying predicate register is addressed. If the qualifying predicate is set to 0, then the instruction will not be executed, when the default is to execute anything that is selected for execution.

70. Referring to claim 19, Intel has taught a method as described in claim 11. Intel has further taught that bits 1:0 specify a context associated with a control and status register (CSR) reference. See page C-4 and note that the values of bits 1:0 will specify a certain qualifying predicate register. If the qualifying predicate is set to 0, then the instruction will not be executed, when the default is to execute anything that is selected for execution.

71. Referring to claims 26 and 29-38, claims 26 and 29-38 are rejected for the same reasons set forth in the rejection of claims 7 and 10-19, respectively, because Intel has taught instructions stored on a medium for performing the method of claims 7 and 10-19.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
September 16, 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100